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FOR

COMPOSITE GROUND SHIELD FOR PASSIVE COMPONENTS IN A SEMICONDUCTOR DIE

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BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention is generally in the field of semiconductors. More specifically, the invention is in the field of ground shields in semiconductor dies.

2. RELATED ART

Accurate modeling of passive components, such as inductors, in a circuit design requires a clearly defined AC ground. This AC ground can be defined by using substrate contacts, which can be formed close to the passive component, or a metal or polysilicon ground shield situated below the passive component. The substrate contacts and ground shield can be electrically connected to a ground in an interconnect metal layer, such as interconnect metal layer one, i.e. "M1," in a semiconductor die. For an inductor, a ground shield can cause a desirable increase in the inductor's quality factor ("Q") while causing an undesirable increase in the inductor's capacitance, which can decrease the usable range of the inductor. By way of background, a ground shield causes a capacitance effect on an inductor that is inversely proportional to the distance between the interconnect metal layer that the inductor is fabricated in and the ground shield. In contrast to a ground shield, substrate contacts situated close to the inductor yield a lower increase in the inductor's Q while causing a less severe capacitance effect.

The use of a metal shield, which can be patterned in M1, or a polysilicon shield have been suggested to obtain an inductor having an higher quality factor ("Q"). However, a metal shield formed in M1 can severely degrade the usable frequency range or self resonance frequency ("SRF") of an inductor by as much as 30 %. Although a

polysilicon shield causes only approximately one half of the SRF degradation caused by the metal shield, the Q of the inductor that is obtainable with the polysilicon shield is lower than the Q that can be realized with the metal shield.

Thus, there is a need in the art for a more effective ground shield for a passive component, such as an inductor, fabricated in a semiconductor die.

SUMMARY OF THE INVENTION

The present invention is directed to composite ground shield for passive components in a semiconductor die. The present invention addresses and resolves the need in the art for a more effective ground shield for a passive component, such as an inductor, fabricated in a semiconductor die.

According to one exemplary embodiment, a structure situated in a semiconductor die comprises an active shield situated in a substrate, where the active shield comprises a salicide layer situated on an active region, and where the active shield has a first conductivity type. The salicide layer may comprise titanium silicide, cobalt silicide, and nickel mono-silicide, for example. The active shield can further comprise a plurality of fingers, where each of the plurality of fingers comprises a salicide segment situated on an active segment. The active shield can be situated in a well in the substrate, where the well is connected to a voltage source greater than or equal to a ground voltage and having no AC component, and where the well has a second conductivity type.

According to this exemplary embodiment, the structure further comprises a passive component situated in an interconnect metal layer in the semiconductor die, where the passive component is situated above the active shield, and where the active shield defines an AC ground for the passive component. The passive component can be an inductor, for example. The structure further comprises at least one contact, where the at least one contact connects the active shield to a semiconductor die AC ground. The structure can further comprise a salicided active region situated adjacent to at least one side of the active shield, where the salicided active region has the second conductivity

type. Other features and advantages of the present invention will become more readily apparent to those of ordinary skill in the art after reviewing the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates a top view of an exemplary structure including an exemplary composite ground shield in accordance with one embodiment of the present invention.

Figure 1B illustrates a cross sectional view of the exemplary structure in Figure 1A.

Figure 2 illustrates a top view of an exemplary structure including an exemplary inductor situated over an exemplary active shield in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to composite ground shield for passive components in a semiconductor die. The following description contains specific information pertaining to the implementation of the present invention. One skilled in the art will recognize that the present invention may be implemented in a manner different from that specifically discussed in the present application. Moreover, some of the specific details of the invention are not discussed in order not to obscure the invention.

The drawings in the present application and their accompanying detailed description are directed to merely exemplary embodiments of the invention. To maintain brevity, other embodiments of the present invention are not specifically described in the present application and are not specifically illustrated by the present drawings.

Figure 1A shows a top view of a portion of a semiconductor die including an exemplary composite ground shield in accordance with one embodiment of the present invention. Certain details and features have been left out of Figure 1A, which are apparent to a person of ordinary skill in the art. As shown in Figure 1A, structure 100 includes substrate 102, well 104, and composite ground shield 105, which includes salicided active region 106 and active shield 108. Active shield 108 further includes finger regions 110a, 110b, 110c, and 110d and segments 112a, 112b, 112c, and 112d. Finger region 110a further includes fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g.

Also shown in Figure 1A, well 104 is situated in substrate 102. Substrate 102 can be lightly doped with a P type dopant to form a substrate having P type conductivity, i.e. a P substrate. In the present embodiment, well 104 can be lightly doped with an N type

dopant to form a well having N type conductivity, i.e. an N well. In one embodiment, well 104 can be a P well, i.e. it can be lightly doped with a P type dopant. Further shown in Figure 1A, active shield 108 is situated in well 104. Active shield 108 includes finger regions 110a, 110b, 110c, and 110d, which are connected to active shield segments 112a, 112b, 112c, and 112d, respectively. Active shield segments 112a, 112b, 112c, and 112d extend along sides 116a, 116b, 116c, and 116d of active shield 108, respectively. Active shield segments 112a and 112c include gaps 113a and 113b, respectively, which can prevent magnetically induced eddy currents from a passive component, such as an inductor, a transformer, or a balun, situated above active shield 108 from forming a closed current loop. Finger region 110a includes fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g, which extend from active shield segment 112a toward the center of active shield 108, as indicated by arrow 118.

As shown in Figure 1A, finger 114d, which is the longest finger in finger region 110a, extends from the approximate center of active shield segment 112a to the approximate center of active shield 108. Fingers 114c and 114e, which are shorter than finger 114d, i.e. they do not extend as far toward the center of active shield 108 as finger 114d, are situated along respective sides of finger 114d. Fingers 114b and 114f, which are shorter than fingers 114c and 114e, are situated along respective sides of fingers 114c and 114e, and fingers 114a and 114g, which are the shortest fingers in finger region 110a, are situated along respective sides of fingers 114b and 114f.

Finger regions 110b, 110c, and 110d each comprise a group of fingers, such as fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g, which extend from respective

active shield segments 112b, 112c, and 112d toward the center of active shield 108. As a result, the group of fingers in each of finger regions 110a and 110c are situated perpendicular to the group of fingers in each of finger regions 110b and 110d. It is noted that only fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g in finger region 110a are specifically discussed in the present application to preserve brevity.

In the present embodiment, active shield 108 comprises a P type active region (not shown in Figure 1A), which is situated in well 104, and salicide layer 120, which is situated on the P type active region (not shown in Figure 1A). Thus, active shield 108 is a P type active shield. In an embodiment in which well 104 is a P well, active shield 108 can be an N type active shield, which can comprise a silicide layer situated over an N type active region. Active shield 108, including finger regions 110a, 110b, 110c, and 110d and active shield segments 112a, 112b, 112c, and 112d, can be formed by appropriately patterning silicon in substrate 102 to form a patterned silicon region. The patterned silicon region can be implanted with a P type dopant to form a P type active region, which is situated in well 104.

A mask can then be formed over the wafer to protect portions of the wafer from a subsequent silicide process, while leaving P type active region exposed, i.e. unmasked. Next, a salicide layer, i.e. salicide layer 120, can be formed on the exposed P type active region by using a salicide process. By way of background, salicide is the process of forming self-aligned silicide. In the salicide process, the entire wafer is covered with metal, such as titanium, cobalt, nickel, or other appropriate metal, and silicide is formed only where silicon is exposed. Salicide layer 120 can comprise titanium silicide ("$TiSi_2$"),

cobalt silicide ("$CoSi_2$"), nickel mono-silicide ("NiSi"), or other appropriate silicide.

Further shown in Figure 1A, contacts 122 are situated on active shield segments 112a, 112b, 112c, and 112d and electrically connect active shield 108 to a feed line (not shown in Figure 1A) in interconnect metal layer one, i.e. M1. The M1 feed line (not shown in Figure 1A) can be connected to ground in the semiconductor die. Thus, contacts 122 electrically connect active shield 108 to the semiconductor die ground. Also shown in Figure 1A, salicided active region 106 is situated in well 104 and also situated along sides 116a, 116b, 116c, and 116d of active shield 108 such that salicided active region 106 surrounds active shield 108. In other embodiments, salicided active region 106 may be situated along one, two, or three sides of active shield 108. Salicided active region 106 is appropriately separated from active shield 108 by distance 124. In the present embodiment, salicided active region 106 comprises an N type active region (not shown in Figure 1A), which is situated in well 104, and salicide layer 126, which is situated on the N type active region (not shown in Figure 1A). Salicided active region 106 includes gaps 107a and 107b which can prevent magnetically induced eddy currents from a passive component, such as an inductor, transformer, or balun, situated above active shield 108 from forming a closed current loop.

Salicided active region 106 can be formed by appropriately patterning silicon in well 104 and heavily doping the patterned silicon with an N type dopant. A salicide process can then be used to form a salicide layer, i.e. salicide layer 126, on the N type active region and complete the formation salicided active region 106. Salicide layer 126 is substantially similar in composition to salicide layer 120. Thus, since salicided active

region 106 and well 104 each have N type conductivity, salicided active region 106 forms an ohmic contact with well 104.

Further shown in Figure 1A, contacts 128 are situated on salicided active region 106 and can be connected to a feed line (not shown in Figure 1A) in M1. The feed line (not shown in Figure 1A) in M1 can be connected to a voltage source greater than or equal to ground and having no AC component, such as Vdd. In an embodiment in which active shield 108 is an N type active shield, well 104 is a P well, and salicided active region 106 comprises a P type active region, contacts 128 can electrically connect well 104 to ground.

Figure 1B shows a cross-sectional view of structure 100 in Figure 1A along line 1B-1B in Figure 1A. In particular, substrate 102, well 104, composite ground shield 105, salicided active region 106, active shield 108, finger region 110a, active shield segments 112b and 112d, fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g, and salicide layer 126 correspond to the same elements in Figure 1A and Figure 1B. Fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g include salicide segments 130a, 130b, 130c, 130d, 130e, 130f, and 130g and active segments 132a, 132b, 132c, 132d, 132e, 132f, and 132g, respectively. Active shield segments 112b and 112d include active segments 134a and 134b and salicide segments 136a and 136b, respectively, and salicided active region 106 includes active region 138 and salicide layer 126.

As shown in Figure 1B, active segments 132a, 132b, 132c, 132d, 132e, 132f, 132g and 134a and 134b are situated in well 104 and comprise silicon that is heavily doped with a P type dopant. Also shown in Figure 1B, active region 138 is situated in well 104

and comprises silicon that is heavily doped with an N type dopant. In an embodiment in which well 104 is a P well and active shield 108 is an N type active shield, active segments 132a, 132b, 132c, 132d, 132e, 132f, 132g and 134a and 134b comprise silicon that is heavily doped with an N type dopant, and active segments 134a and 134 can comprise silicon that is heavily doped with a P type dopant.

Also shown in Figure 1B, salicide segments 130a, 130b, 130c, 130d, 130e, 130f, and 130g and 136a and 136b, which form a portion of salicide layer 120 in Figure 1A, are situated on active segments 132a, 132b, 132c, 132d, 132e, 132f, 132g and 134a and 134b, respectively. Salicide segments 130a, 130b, 130c, 130d, 130e, 130f, and 130g and 136a and 136b reduce the resistance of fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g and active shield segments 112b and 112d, respectively. Further shown in Figure 1B, salicide layer 126 is situated on active region 138 and provides reduced resistance in salicided active region 106. Also shown in Figure 1B, distance 140 indicates the spacing between fingers, such as fingers 114a and 114b. Distance 140 can be appropriately adjusted to provide a minimal separation distance between adjacent fingers in finger regions 110a, 110b, 110c, and 110d in Figure 1A.

Figure 2 shows a top view of a portion of a semiconductor die including an exemplary inductor situated over an exemplary active shield in accordance with one embodiment of the present invention. In Figure 2, active shield 208, finger regions 210a, 210b, 210c, and 210d, active shield segments 212a, 212b, 212c, and 212d, and contacts 222 in structure 200 correspond, respectively, to active shield 108, finger regions 110a, 110b, 110c, and 110d, active shield segments 112a, 112b, 112c, and 112d, and contacts

122 in structure 100 in Figure 1A. Structure 200 also includes dielectric layer 250 and inductor 252.

As shown in Figure 2, inductor 252 is situated on dielectric layer 250 and includes interconnect metal segments 254a, 254b, 254c, 254d, 254e, 254f, and 254g and terminals 256a and 256b. Inductor 252 is a square spiral inductor having winding pattern that comprises interconnect metal segments 254a, 254b, 254c, 254d, 254e, 254f, and 254g. Inductor 252 can be situated in the top interconnect metal layer in the semiconductor die, such as interconnect metal layer six, i.e. "M6," and can be formed by appropriately patterning and etching a layer of interconnect metal. In other embodiments, inductor 252 can have an octagonal, circular, or rectangular shape. Terminals 256a and 256b are connected to interconnect metal segments 254a and 254g, respectively. Inductor 252 is also situated over active shield 208.

In particular, interconnect metal segments 254a and 254e are situated over finger region 210d, interconnect metal segments 254b and 254f are situated over finger region 210c, interconnect metal segments 254c and 254g are situated over finger region 210b, and interconnect metal segment 254d is situated over finger region 210a. Also, the fingers in each respective finger region are situated perpendicular to the interconnect metal segment(s) that are situated over the respective finger region. For example, the fingers in finger region 210a, such as fingers 114a, 114b, 114c, 114d, 114e, 114f, and 114g in Figure 1A, are situated perpendicular to interconnect metal segment 254d. Thus, since each interconnect metal segment in the winding pattern of inductor 252 is situated perpendicular to fingers in the particular finger region that is situated under the

interconnect metal segment, image currents are prevented from being induced in the finger regions of the active shield, such as finger regions 210a, 210b, 210c, and 210d, by the magnetic field of inductor 252.

The operation of the present invention's composite ground shield will now be discussed in relation to Figures 1A, 1B, and 2. Active shield 108 in Figures 1A and 1B can be situated under a passive component, such as inductor 252 in Figure 2, which can be situated in M6. In other embodiments, the passive component can be a transformer or a balun. Since active shield 108 is electrically connected to ground in the semiconductor die by contacts 122 and a feed line in M1 (not shown in any of the figures), active shield 108 provides a clearly defined AC ground for inductor 252. Thus the fingers in the finger regions of active shield 108, such as fingers 114a and 114b in finger region 110a, can effectively terminate the electric field generated by inductor 252. As a result of effectively terminating the electric field generated by inductor 252, the Q of inductor 252 is increased.

Also, since active shield 108 is formed in a salicided active region in well 104, it, i.e. active shield 108, is situated a greater distance from inductor 252 compared to a conventional ground shield, which is situated in either M1 or polysilicon. By way of example, a conventional ground shield situated in polysilicon can be between approximately 2.0 % and approximately 3.0 % closer to inductor 252 (as situated in M6) compared to active shield 108, which is situated in an active region in well 104. By way of further example, a conventional ground shield situated in M1 can be approximately 10.0 % closer to inductor 252 (as situated in M6) compared to active shield 108. As

discussed above, a ground shield causes a capacitance effect on an inductor that is inversely proportional to the distance between the interconnect metal layer that the inductor is fabricated in and the ground shield. Thus, by forming an active shield in a salicided active region, the present invention advantageously achieves an active shield having a reduced capacitance effect on an inductor situated above the active shield compared to a conventional ground shield.

Additionally, the present invention's composite ground shield, i.e. composite ground shield 105, provides salicided active region 106, which surrounds active shield 108, has N type conductivity, and is situated in an N well, i.e. well 104. Since active shield 108 is a P type active shield, a "PN" junction is formed between active shield 108 and well 104. Thus, by connecting salicided active region 106 to a voltage source greater than or equal to ground and having no AC component, the "PN" junction is reverse or zero biased, which minimizes leakage current flowing between active shield 108 and well 104. Additionally, any RF noise injected into well 104 by inductor 252 will be shunted to AC ground.

Also, since substrate 102 is a P type substrate in the present embodiment, a "PN" junction is formed between substrate 102 and well 104, which is also reverse or zero biased by connecting salicide active region 106 to a voltage source greater than or equal to ground and having no AC component. Thus, the "PN" junction formed between substrate 102 and well 104 provides additional noise isolation. However, not connecting the well, i.e. well 104, and leaving it floating will not impair the function of the shield, i.e. active shield 108. In the present embodiment, substrate 102 is not connected to a

voltage source, i.e. it is left floating. In one embodiment, substrate 102 may be connected by an ohmic contact to a voltage source greater than or equal to ground voltage, i.e. "ground," and having no AC component, which provides an additional path for shunting RF noise in substrate 102 to AC ground.

In one embodiment, active shield 108 is an N type active shield, well 104 is a P well, substrate 102 is a P substrate, and salicided active region 106 has P type conductivity and forms an ohmic contact with well 104. In that embodiment, the "PN" junction formed between the P well and the N type active shield can be zero biased by connecting the P well to a voltage source equal to ground through salicided active region 106, which minimizes leakage current in the P well and also shunts RF noise in the P well or P substrate to AC ground. In other embodiments, active shield 108 and well 104 can have the same conductivity type. For example, active shield 108 and well 104 can both have N type conductivity or they, i.e. active shield 108 and well 104, can both have P type conductivity.

In another embodiment, active shield 108 can be formed directly in a substrate without utilizing a well, such as well 104. In such embodiment, active shield 108 and the substrate would have an opposite conductivity type. For example, if active shield 108 were formed in a P type substrate, active shield 108 would be an N type active shield, and if active shield 108 were formed in an N type substrate, active shield 108 would be a P type active shield.

Thus, as discussed above, by forming a composite ground shield in a salicided active region in a well, the present invention advantageously achieves a composite ground

shield that clearly defines an AC ground for a passive component, such as an inductor, situated above the composite ground shield, while providing a reduced capacitance effect on the inductor compared to a conventional ground shield. Furthermore, by integrating a salicided active region with an active shield in a composite ground shield, the present invention advantageously minimizes leakage current between the active shield and the well in which the active shield is situated while shunting RF noise in the well or substrate to AC ground.

From the above description of the invention it is manifest that various techniques can be used for implementing the concepts of the present invention without departing from its scope. Moreover, while the invention has been described with specific reference to certain embodiments, a person of ordinary skill in the art would appreciate that changes can be made in form and detail without departing from the spirit and the scope of the invention. Thus, the described embodiments are to be considered in all respects as illustrative and not restrictive. It should also be understood that the invention is not limited to the particular embodiments described herein but is capable of many rearrangements, modifications, and substitutions without departing from the scope of the invention.

Thus, composite ground shield for passive components in a semiconductor die has been described.